IN THE CLAIMS

1.-4. (Canceled)

5. (Currently Amended) A bimodal power data link transceiver device, the device comprising:

a transceiver integrated circuit (IC), the transceiver IC comprising:

a transmitter, the transmitter having;

~~a phase locked loop (PLL) frequency synthesizer comprising a~~ partial ~~first~~ voltage controlled oscillator (VCO) designed to accept at least one input from frequency setting components external to the transceiver IC and in combination with the frequency setting components to produce a first clock signal at a first frequency set by the frequency setting components;

a first power amplifier, the first power amplifier coupled to the ~~PLL frequency synthesizer~~partial VCO; and

a receiver;

a second power amplifier coupled to the first power amplifier;

a transmit/receive switch coupled to the second power amplifier and the receiver;

a controller coupled to the transceiver IC;

a direct digital frequency synthesizer having an output coupled to an input of the transceiver IC;

a ~~second~~ complete voltage controlled oscillator (VCO) coupled to the partial ~~first~~ VCO, the complete VCO configured to produce a second clock signal at a second frequency and to couple the second clock signal to the partial VCO, the complete VCO further configured to utilize the partial VCO as one of an emitter follower circuit, a buffer, or a filter; and

a loop filter coupled to the ~~second~~ complete VCO and the transceiver IC.

6. (Currently Amended) A bimodal power data link transceiver device as in claim 5, wherein the partial VCO, complete VCO, and the loop filter form part of a phase locked loop (PLL), wherein the PLL ~~frequency synthesizer~~ and the transceiver IC further ~~comprises~~comprise:

a phase detector coupled to the loop filter; and

a crystal oscillator coupled to the phase detector.

7. (Original) A bimodal power data link transceiver device as in claim 5, wherein the receiver comprises:

a low noise amplifier;

a quadrature mixer pair, the quadrature mixer pair coupled to the low noise amplifier and the PLL frequency synthesizer, the quadrature mixer pair having:

a first quadrature signal;

a second quadrature signal;

a demodulator;

a first signal channel, the first signal channel coupling the first quadrature signal to the demodulator; and

a second signal channel, the second signal channel coupling the second quadrature signal to the demodulator.

8. (Original) A bimodal power data link transceiver device as in claim 5, wherein the transceiver IC comprises at least one field programmable gate array (FPGA).

9. (Original) A bimodal power data link transceiver device as in claim 5 wherein the transmit/receive switch comprises a plurality of diodes.

10. (Currently Amended) A method for transceiving data in a device adapted to transceive data in the radio frequency spectrum, the method comprising:

providing a transceiver integrated circuit (IC), the transceiver IC having:

a partial ~~first~~ voltage controlled oscillator (VCO) designed to accept at least one input from frequency setting components external to the transceiver IC and in combination with the frequency setting components to produce a first clock signal at a first frequency set by the frequency setting components;

an oscillator input port coupled to the partial ~~first~~ VCO;

a frequency reference port;

a radio frequency input port;

a radio frequency output port;

a phase detector output port;

using a ~~second~~ complete VCO, generating a VCO signal for input to the oscillator input port, the VCO signal comprising a second clock signal at a second frequency,

the complete VCO configured to utilize the partial VCO as one of an emitter follower circuit, a buffer, or a filter;

coupling a direct digital synthesizer (DDS) to the frequency reference port;

coupling the radio frequency output port to a power amplifier; and

coupling the radio frequency input port to a transmit/receive switch.

11. (Previously Presented) A method as in claim 10 wherein providing a transceiver IC further comprises:

providing a field programmable gate array (FPGA);and

programming the FPGA to operate as a transceiver.

12. (Currently Amended) A method as in claim 10 wherein the step of generating a ~~voltage controlled oscillator~~VCO signal for input to the oscillator port further comprises;

coupling the phase detector output port to at least one loop filter; and

coupling the at least one loop filter to the ~~second~~ complete VCO.

13. (Previously Presented) A method as in claim 10 wherein coupling a DDS to the frequency reference port further comprises coupling a first microprocessor controller to the DDS.

14. (Previously Presented) A method as in claim 13 wherein coupling the first microprocessor controller to the DDS further comprises setting a center transmit frequency.

15. (Previously Presented) A method as in claim 13 wherein coupling the first microprocessor controller to the DDS further comprises modulating a transmit frequency.

16. (Previously Presented) A method as in claim 10 further comprising:

operating the device in a quiescent baseline receiver mode, wherein the quiescent baseline receiver mode comprises a first power mode;

operating the device in a burst transmit mode when not in the quiescent baseline receiver mode, wherein the burst transmit mode comprises a second power mode, wherein the second power mode is greater than the first power mode;

operating the device with a transmit/receive time ratio less than 1.5; and

transceiving a RF carrier frequency less than 200 MHz.

17. (Previously Presented) A method as in claim 10 further comprising operating the device with a global positioning indicator.

18. (Original) A method as in claim 10 further comprising transceiving data in weapons munitions, wherein transceiving data in weapons munitions further comprises transmitting frequency shift key (FSK) modulated signals.

19. (Original) A method as in claim 10 further comprising transceiving data in a landmine.

20. (Currently Amended) A bimodal power data link transceiver device, the device comprising:

a receiver section;

a transmitter section;

a phased locked loop (PLL) frequency generator section, wherein the PLL frequency generator section comprises:

a ~~first~~ complete voltage controlled oscillator (VCO);

an integrated circuit (IC), wherein the integrated circuit comprises:

a ~~first~~ buffer, wherein the buffer is coupled to the ~~first~~ complete VCO, and wherein the ~~first~~ buffer comprises:

a partial ~~second~~ VCO designed to accept at least one input from frequency setting components external to the transceiver IC and in combination with the frequency setting components to produce a first clock signal at a first frequency set by the frequency setting components, wherein the complete VCO is configured to produce a second clock signal at a second frequency and to couple the second clock signal to the partial VCO, the complete VCO further configured to utilize the partial VCO as the buffer,

a digital direct synthesizer (DDS), wherein the DDS is coupled to the IC; and

a controller section, the controller section coupled to the PLL frequency generator section and the receiver section.

21. (Original) A bimodal power data link transceiver device as in claim 20, wherein the transmitter section comprises:

the IC, the IC further comprising:

a first amplifier, wherein the first amplifier is coupled to the PLL frequency generator section; and

a second amplifier, the second amplifier coupled to the first amplifier.

22. (Original) A bimodal power data link transceiver device as in claim 20, wherein the receiver section comprises:

a low noise amplifier;

a quadrature mixer pair coupled to the low noise amplifier; and

a demodulator coupled to the quadrature mixer pair.

23. (Original) A bimodal power data link transceiver device as in claim 20, wherein the device is adapted to fit in a weapon.

24. (Original) A bimodal power data link transceiver device as in claim 23 wherein the weapon comprises a landmine.

25. (Original) A bimodal power data link transceiver device as in claim 23 wherein the weapon comprises a sea mine.

26. (Currently Amended) A bimodal power data link transceiver device as in claim 5, wherein the transceiver IC is configured to operate at and above a first frequency and wherein the ~~second~~ complete VCO is configured to operate the transceiver IC at a second frequency smaller than the first frequency.

27. (Currently Amended) A method as in claim 10, wherein the transceiver IC is ~~configured~~ designed to operate at and above ~~a~~ the first frequency and wherein ~~generating a VCO signal further comprising using the second VCO to generate the VCO signal at a second frequency at which the transceiver IC operates,~~ the second frequency is smaller than the first frequency.

28. (Currently Amended) A bimodal power data link transceiver device as in claim 20, wherein the integrated circuit is configured to operate at and above ~~a~~ the first frequency, ~~wherein the first VCO is configured to operate the transceiver IC at a second frequency,~~ and wherein the second frequency is smaller than the first frequency.

29. (Currently Amended) A bimodal power data link transceiver device, the device comprising:

a transceiver integrated circuit (IC) ~~configured~~ designed to operate at and above a first frequency, the transceiver IC comprising:

a transmitter, the transmitter having:

a partial ~~first~~ voltage controlled oscillator (VCO) designed to accept at least one input from frequency setting components external to the transceiver IC and in combination with the frequency setting components to produce a first clock signal at the first frequency set by the frequency setting components;

a first power amplifier, the first power amplifier coupled to the partial ~~first~~ VCO; and

a receiver coupled to the partial ~~first~~ VCO,

a second power amplifier coupled to the first power amplifier;

a transmit/receive switch coupled to the second power amplifier and the receiver;

a controller coupled to the transceiver IC;

a direct digital frequency synthesizer coupled to the controller and having an output coupled to an input of the transceiver IC;

a complete~~second~~ voltage controlled oscillator (VCO) coupled to the partial ~~first~~ VCO, wherein the ~~second~~ complete VCO is configured to operate the transceiver IC at a second frequency smaller than the first frequency, the complete VCO configured to produce a second clock signal at the second frequency, the complete VCO further configured to utilize the partial VCO as one of an emitter follower circuit, a buffer, or a filter; and

a loop filter coupled to the ~~second~~ complete VCO and the transceiver IC.

30. (Canceled)

31. (Previously Presented) The device of claim 29, wherein the first frequency is 300 megahertz (MHz) and the second frequency is 200 MHz.